REMARKS

Applicant is in receipt of the Office Action mailed October 18, 2006. Claims 2, 8, 11, 25, 29, 33, and 37 have been cancelled. Claims 1, 3, 9, 10, 23, 26, 28, 30, 32, 34-36, and 38 have been amended. Claims 1, 3-7, 9-10, 12-24, 26-28, 30-32, 34-36, and 38-39 are pending in the case. Reconsideration of the present case is earnestly requested in light of the following remarks.

Double Patenting Rejection

Claim 6 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 85 of U.S. Patent No. 7,024,660 ("'660"), specifically, that claim 85 of '660 anticipates the features and limitations of claim 6. Applicant respectfully disagrees.

Claim 6 and its base claim 1 (amended) recite:

1. A memory medium comprising program instructions for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, wherein the program instructions are executable to perform:

a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

b) configuring the programmable hardware element with the first hardware configuration program;

c) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing;

d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program; and

repeating a) – d) one or more times in an iterative manner, wherein for one or more iterations the first portion of the program is a successively larger portion of the program.

6. The memory medium of claim 1, wherein the programmable hardware element is coupled to one or more hardware resources, and wherein said executing further comprises:

invoking the one or more hardware resources to perform the function.

Claim 85 of '660 (formatted for clarity) recites:

85. A memory medium comprised in a computer system, comprising:

a user interface program which is executable to receive user input specifying a function;

a configuration generation program which is executable to generate a hardware configuration program based on the user input, where the hardware configuration program is deployable on a programmable hardware element, and wherein the hardware configuration program specifies a configuration for the programmable hardware element that implements the function, and wherein the hardware configuration program further specifies usage of one or more fixed hardware resources by the programmable hardware element in performing the function; and

a test configuration;

a deployment program executable to deploy the test configuration onto the programmable hardware element, wherein, after configuration with the test configuration, the programmable hardware element provides for communication between the one or more fixed hardware resources and the program;

wherein, for debugging purposes, the program is executable by a processor in the computer system to test performance of the function including the usage of the one or more fixed hardware resources, wherein during execution the program communicates

with the one or more fixed hardware resources through the programmable hardware element.

As the Examiner is certainly aware, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant respectfully notes that in claim 85 of '660, the program (the hardware configuration program for implementing the function) is executed on the processor of the computer system, communicating with the fixed hardware resources via the test configuration deployed and implemented on the programmable hardware element.

In contrast, in claim 6 (plus claim 1), the programmable hardware element executes a first portion of the program, and the computer system (processor) executes the remaining portion of the program for debugging purposes, where one or more hardware resources coupled to the programmable hardware element are invoked to perform the function.

While '660 claim 85 has some similarities with respect to claim 6 (plus claim 1), Applicant respectfully submits that claim 85 fails to teach or suggest all the features and limitations of claim 6 (plus 1).

For example, nowhere does claim 85 teach or suggest **converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user**, as recited in claim 1. Nor does claim 85 teach or suggest **the programmable hardware element executing the first portion of the program; and the computer system executing the remaining portion of the program; wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing**.

Applicant respectfully submits that the Examiner has mischaracterized at least some portions of claim 85. For example, the Examiner asserts equivalence between "the program" of claim 85, and the "remaining portion" of the program of claim 6, which is improper, as these terms (and concepts) are not interchangeable. For example, if the remaining portion were in fact, "the program", there would be no first portion implemented on the programmable hardware element, and so the system would no longer be the system claimed.

Moreover, Applicant respectfully notes that there is substantial difference between executing an entire program on a computer system that communicates with fixed hardware resources through a test configuration implemented on a programmable hardware element; and executing a first *portion* of a program on a programmable hardware element, and a remaining *portion* of the program on a computer system, where either or both portions may communicate with fixed hardware resources through the programmable hardware element. Note that in the latter case, execution of the program, which is distributed between the programmable hardware element and the computer system, involves coordinated execution among these distributed portions, including communication by the portions with the fixed hardware resources; whereas in the former case ('660), the program (which is not distributed) is executed only on the computer system, but also communicates with the fixed hardware resources.

Thus, although in both approaches, the program communicates with fixed hardware resources through the programmable hardware element, in '660 claim 85 the program is not distributed, while in claim 6 (plus 1), the program is distributed (over the computer system and the programmable hardware element). Thus, the system of '660 claim 85 is not functionally equivalent to that of claim 6 (plus 1), and so Applicant respectfully submits that '660 claim 85 does not anticipate claim 6 (plus 1) of the present application.

Applicant further submits that '660 claim 85 nowhere teaches or suggests **repeating a) – d) one or more times in an iterative manner, wherein for one or more iterations the first portion of the program is a successively larger portion of the program**, as claimed.

For at least the reasons presented above, Applicant submits that '660 claim 85 fails to anticipate claim 6, and so claim 6 is patentably distinct and non-obvious over claim 85 of '660, and is thus allowable.

Removal of the double patenting rejection of claim 6 is earnestly requested.

Section 102 Rejections

Claims 1-39 were rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al. (USPN: 6,009,256, "Tseng"). Applicant respectfully disagrees.

As noted above, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Again, amended claim 1 recites:

1. A memory medium comprising program instructions for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, wherein the program instructions are executable to perform:

a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

b) configuring the programmable hardware element with the first hardware configuration program;

c) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing;

d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program; and

repeating a) – d) one or more times in an iterative manner, wherein for one or more iterations the first portion of the program is a successively larger portion of the program.

Claims 2, 8, 11, 25, 29, 33, and 37 have been cancelled, thus rendering their rejections moot.

Applicant respectfully submits that Tseng fails to teach or suggest **converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user**, as recited in claim 1, nor **the programmable hardware element executing the first portion of the program; and the computer system executing the remaining portion of the program; wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing**.

Applicant respectfully notes that Tseng is directed to electronic circuit design testing and simulation/emulation using software and hardware based models. Applicant respectfully notes that the circuit design being tested in Tseng, which the Office Action has interpreted as Applicant's program, is *not* intended for deployment to a programmable hardware element, but rather is being modeled to debug the design, after which the circuit will presumably be manufactured. Nowhere does Tseng indicate that the circuit design is intended for deployment on a programmable hardware element (e.g., an FPGA); rather, the circuit design is *modeled* in software and/or hardware, and is intended for deployment as a circuit, e.g., not for deployment to an FPGA.

More specifically, Tseng does not disclose a program intended for deployment on a programmable hardware element where a portion of the program is implemented on the

targeted programmable hardware element, and another portion is executed and debugged on a computer system (but is ultimately intended for deployment on the programmable hardware element). Rather, in Tseng's system, both the software and hardware models are for simulating/emulating an electronic circuit design that is *not* intended for deployment on the hardware (FPGA) used to implement the hardware model.

Tseng's system operates in various modes, which are described by Tseng thusly:

Col. 8:51-58:

> A. SIMULATION/HARDWARE ACCELERATION MODES
>
> The SEmulator system, through automatic component type analysis, can model the user's custom circuit design in software and hardware. The entire user circuit design is modeled in software, whereas evaluation components (i.e., register component, combinational component) are modeled in hardware. Hardware modeling is facilitated by the component type analysis.

As may be seen, in this mode, the entire user circuit design is modeled in software, and evaluation (testing) components for testing the design are modeled or implemented in hardware (FPGA(s)). Nowhere does the text describe Applicant's claimed portions of a program that is intended for deployment on a programmable hardware element being distributed between a computer system and a programmable hardware element, where the portion on the computer system is to be debugged by a user, nor executing the two portions on the programmable hardware element and computer systems, respectively, as claimed. Applicant notes that Tseng's evaluation components for testing the design (which are implemented in hardware) are *not* part of the program proper, as it is with claim 1, but rather are only used for debugging.

Thus, this mode of Tseng does not anticipate these features and limitations of claim 1.

Col. 9:45-53:

> B. EMULATION WITH TARGET SYSTEM MODE
>
> The SEmulation system is capable of emulating the user's circuit within its target system environment. The target system outputs data to the hardware model for evaluation and the hardware model also outputs data to the

> target system. Additionally, the software kernel controls the operation of this mode so that the user still has the option to start, stop, assert values, inspect values, single step, and switch from one mode to another.

As the text indicates, in this mode, the circuit design is modeled (emulated) within its target system environment. The hardware model (implemented on the FPGA(s)) performs evaluation functionality for testing the circuit, and a software kernel (which controls the operation of the entire system) provides a user interface for the testing system. Nowhere does the text describe this mode as including Applicant's claimed portions of a program that is intended for deployment on a programmable hardware element being distributed between a computer system and a programmable hardware element, where the portion on the computer system is to be debugged by a user, nor executing the two portions on the programmable hardware element and computer systems, respectively, as claimed. As noted above, Tseng's models are for debugging a circuit design that is *not* intended for deployment to programmable hardware; rather, the FPGA(s) is *only* used for debugging.

Thus, this mode also does not anticipate these features and limitations of claim 1.

Col. 9:54-67:

> C. POST-SIMULATION ANALYSIS MODE
>
> Logs provide the user with a historical record of the simulation session. Unlike known simulation systems, the SEmulation system does not log every single value, internal state, or value change during the simulation process. The SEmulation system logs only selected values and states based on a logging frequency (i.e., log 1 record every N cycles). During the post-simulation stage, if the user wants to examine various data around point X in the just-completed simulation session, the user goes to one of the logged points, say logged point Y, that is closest and temporally located prior to point X. The user then simulates from that selected logged point Y to his desired point X to obtain simulation results.

As may be seen, this mode is directed to logging selected values and states based on a specified logging frequency. Clearly, this mode similarly fails to anticipate these features and limitations of claim 1.

Col. 10:1-9:

> D. HARDWARE IMPLEMENTATION SCHEMES
>
> The SEmulation system implements an array of FPGA chips on a reconfigurable board. Based on the hardware model, the SEmulation system partitions, maps, places, and routes each selected portion of the user's circuit design onto the FPGA chips. Thus, for example, a 4.times.4 array of 16 chips may be modeling a large circuit spread out across these 16 chips.

As the text clearly shows, this aspect of Tseng is directed to distribution of a hardware model over an array of FPGA chips on a reconfigurable board. Again, nowhere does the text disclose Applicant's claimed portions of a program that is intended for deployment on a programmable hardware element being distributed between a computer system and a programmable hardware element, where the portion on the computer system is to be debugged by a user, nor executing the two portions on the programmable hardware element and computer system, respectively, as claimed. Rather, in this mode of Tseng, the entire circuit model is implemented in FPGAs.

Thus, this aspect of Tseng also does not anticipate these features and limitations of claim 1.

Thus, none of the disclosed modes of Tseng's system and method anticipate the features and limitations of claim 1.

The Office Action asserts that Tseng discloses **a memory medium comprising program instructions for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function**, citing Figures 7-8, col.4:42-50, and Figures 22-33. Applicant respectfully disagrees.

Figures 7 and 8 illustrate connectivity between a plurality of FPGAs, and col.4:42-50 is also directed to such interconnectivity among the FPGAs:

> The hardware logic element also comprises an array or plurality of field programmable devices coupled together. Each field programmable device includes a portion of the hardware model of the circuit and thus, the combination of all the field programmable devices includes the entire hardware model. A plurality of interconnections also couple the portions of the hardware model together. Each interconnection represents a direct connection between any two field programmable devices located in the same row or column. The shortest path between any two field

> programmable devices in the array is at most two interconnections or "hops."

Applicant notes that the subsequent col.4:54-57 discloses modeling the circuit in both software and hardware:

> Another embodiment of the present invention is a system and method of simulating a circuit, where the circuit is modeled in software and at least a portion of the circuit is modeled in hardware.

As noted above, the circuit design being tested in Tseng, which the Office Action has interpreted as Applicant's program, is *not* intended for deployment to a programmable hardware element, but rather is being modeled to debug the design, after which the circuit will presumably be manufactured. Nowhere does Tseng indicate that the circuit design is intended for deployment on a programmable hardware element (e.g., an FPGA); rather, the circuit design is *modeled* in software and/or hardware, and is intended for deployment as a circuit, e.g., not for deployment to an FPGA.

Figures 22-33 are directed to implementing the hardware model of a circuit design on an array of FPGAs for debugging purposes, and nowhere disclose debugging a portion of a program on a computer system, where *the program is intended for deployment on a programmable hardware element to perform a function*, as claimed. In other words, in Tseng, the circuit design may be designed to perform a function, but not as an implementation on an FPGA; rather, a *model* of the circuit is implemented on the FPGA for debugging purposes only. In direct contrast, in Applicant's system as represented in claim 1, the program is intended for deployment to a programmable hardware element, and a portion is implemented on the programmable hardware element, while another portion (also intended for deployment on the programmable hardware element) remains on the computer system for debugging purposes.

Thus, Tseng fails to disclose this feature of claim 1.

Applicant further submits that Tseng nowhere teaches or suggests **repeating a) – d) one or more times in an iterative manner, wherein for one or more iterations the first portion of the program is a successively larger portion of the program**, as recited in amended claim 1.

Nowhere does Tseng disclose performing such converting, configuring, executing, and receiving user input in an iterative fashion. More specifically, Tseng fails to disclose such repeating, where for at least some of the iterations, the first portion of the program is a successively larger portion of the program. In other words, Tseng fails to teach or suggest such iterative debugging, where, as the program is debugged, the (first) portion of the program that is deployed to the programmable hardware element increases, while the remaining portion (executed by the computer system and debugged by the user) decreases. Said another way, in Applicant's invention as represented in claim 1, during the iterative debugging process, as the program is debugged, the debugged portions may be moved from software implementation to hardware implementation, i.e., from the remaining portion to the first portion.

In asserting that Tseng teaches such iteration, the Examiner cites Figures 2, 5, col. 15:34-57, and col.35:65 – col.36:50. However Applicant has reviewed these citations (and Tseng in general) carefully, and can find no description of these features. For example, neither Figure 2 nor Figure 5 discloses the claimed iterative debugging where successive portions of the program are moved from software emulation to hardware deployment as they are debugged.

Col. 15:34-57 describes emulating the circuit in the context of its target system environment. While this text does mention running the emulation multiple times to debug the circuit design, the text fails to disclose moving portions of the program from software emulation to hardware deployment as they are debugged. Rather, as the text describes, "After the emulation with the target system, the user has results that validate the circuit design or reveal non-functional aspects. At this point, the user can simulate/emulate again as indicated at step 135, stop altogether to modify the circuit design, or proceed to integrated circuit fabrication based on the validated circuit design."

Col.35:65 – col.36:50 describes logging operations for Tseng's debugging process, and makes no mention of iterative debugging where successive portions of the program are moved from software emulation to hardware deployment as they are debugged.

Nowhere does Tseng teach or suggest these features and limitations of claim 1.

Thus, for at least the reasons provided above, Applicant respectfully submits that Tseng neither teaches nor suggests all the features and limitations of claim 1, and so claim 1 and those claims dependent therefrom are patentably distinct and non-obvious over the cited art, and are thus allowable.

Independent claims 23, 28, 32, and 36 include similar limitations as claim 1, and so the above arguments apply with equal force to these claims. Thus, for at least the reasons provided above, claims 23, 28, 32, and 36, and those claims respectively dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Independent claim 27 also recites limitations similar to those of claim 1, although in a slightly different form. More specifically, claim 27 explicitly recites two iterations of the iterative debugging process, where, as in claim 1, the program is partitioned into two portions, a first portion directed to a programmable hardware element, and a first remaining portion directed to a computer system for debugging by the user. The program is executed, including the programmable hardware element executing the first portion of the program, and the computer system executing the first remaining portion of the program. The remaining portion of the program is analyzed and debugged, e.g., by the user. After the user has debugged (modified) the remaining portion (in response to executing the portions on the programmable hardware element and computer system, respectively), the user repartitions the program, specifying a second portion for deployment on the programmable hardware element that includes the first portion and a debugged portion of the first remaining portion of the program, and a second remaining portion that includes only a subset of the first remaining portion of the program. The second portion is then converted and deployed to the programmable hardware element, and the program executed, where the second portion is executed on the programmable hardware element, and the second remaining portion is executed by the computer system.

Nowhere does Tseng teach or suggest these features and limitations. Thus, for at least the reasons provided above, Applicant respectfully submits that Tseng neither teaches nor suggests all the features and limitations of claim 27, and so claim 27 and those claims dependent therefrom are patentably distinct and non-obvious over the cited art, and are thus allowable.

Removal of the section 102 rejection of claim 1, 3-7, 9-10, 12-24, 26-28, 30-32, 34-36, and 38-39 is earnestly requested.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5150-79600/JCH.

Also filed herewith are the following items:

☐ Request for Continued Examination

☐ Terminal Disclaimer

☐ Power of Attorney By Assignee and Revocation of Previous Powers

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,

/Jeffrey C. Hood/

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